AMENDMENTS TO THE CLAIMS

1.-20. (Canceled).

21. (Amended) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide material disposed in the second window over the layer of the second conductive material; and

a second line formed of a conductive material and disposed over the layer of chalcogenide material.

22. (Canceled).

23. (Amended) The memory cell, as set forth in claim 21, wherein the layer of a second conductive material is ~~deposited on the first line using~~ an immersion plated layer ~~plating technique.~~

24. (Original) The memory cell, as set forth in claim 21, wherein the second conductive material comprises at least one of silver and gold.

25. (Original) The memory cell, as set forth in claim 21, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

26. (Amended) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line;

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide material disposed in the second window over the layer of the second conductive material; and

a second line formed <u>of a conductive material and disposed</u> over the layer of chalcogenide material and over the first layer of conductive material.

27. (Canceled).

28. (Amended) The memory cell, as set forth in claim 26, wherein the layer of a second conductive material is ~~deposited on the first line using~~ an immersion plated layer ~~plating technique~~.

29. (Original) The memory cell, as set forth in claim 26, wherein the second conductive material comprises at least one of silver and gold.

30. (Original) The memory cell, as set forth in claim 26, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

31. (Amended) A memory device comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line ~~formed over a substrate~~ disposed in the first window ~~over~~, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide disposed in the second window over the layer of the second conductive material; and

a second line formed of a conductive material and disposed over the layer of chalcogenide.

32.-34. (Canceled).

35. (Amended) The memory device, as set forth in claim 31, wherein the layer of a second conductive material is ~~deposited on the first line using~~ an immersion plated layer ~~plating technique~~.

36. (Amended) The memory device, as set forth in claim 31, wherein the second conductive material comprises at least one of silver and gold.

37. (Amended) The memory device, as set forth in claim 31, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

38. (Amended) An electronic device comprising:

a processor; and

a memory operatively coupled to the processor, the memory comprising a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line ~~formed over a substrate~~ disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide disposed in the second window over the layer of the second conductive material; and

a second line formed of a conductive material and disposed over the layer of chalcogenide.

39.-41. (Canceled).

42. (Amended) The electronic device, as set forth in claim 38, wherein the layer of a second conductive material is ~~deposited on the first line using~~ an immersion plated layer ~~plating technique~~.

43. (Previously Amended) The electronic device, as set forth in claim 38, wherein the second conductive material comprises at least one of silver and gold.

44. (Previously Amended) The electronic device, as set forth in claim 38, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

45.-83. (Canceled).

84. (Previously added) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window formed therein;

a first memory access line disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed in the second window on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material.

85. (Previously added) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first memory access line disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line;

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of

dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed in the second window on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material and over the first layer of conductive material.

86. (Amended) A memory device comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window formed therein;

a first memory access line ~~formed over a substrate~~ disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed on the layer of the second conductive material, wherein the variable resistance material is capable of

changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance.

87.-88. (Canceled).

89. (Amended) An electronic device comprising:

a processor; and

a memory operatively coupled to the processor, the memory comprising a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window formed therein;

a first memory access line ~~formed over a substrate~~ disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance.

90. (New) A memory device comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line;

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide material disposed in the second window over the layer of the second conductive material; and

a second line formed of a conductive material and disposed over the layer of chalcogenide material and over the first layer of conductive material.

91. (New) The memory cell, as set forth in claim 90, wherein the layer of a second conductive material is an immersion plated layer.

92. (New) The memory cell, as set forth in claim 90, wherein the second conductive material comprises at least one of silver and gold.

93. (New) The memory cell, as set forth in claim 90, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

94. (New) An electronic device comprising:

a processor; and

a memory operatively coupled to the processor, the memory comprising a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel, and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line;

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide material disposed in the second window over the layer of the second conductive material; and

a second line formed of a conductive material and disposed over the layer of chalcogenide material and over the first layer of conductive material.

95. (New) The memory cell, as set forth in claim 94, wherein the layer of a second conductive material is an immersion plated layer.

96. (New) The memory cell, as set forth in claim 94, wherein the second conductive material comprises at least one of silver and gold.

97. (New) The memory cell, as set forth in claim 94, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

98. (New) A memory device comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first memory access line disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line;

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window

on the first line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed in the second window on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material and over the first layer of conductive material.